

Modeling router hotspots on network-on-chip

Abstract

A Network-on-Chip (NoC) is a new paradigm in complex System-on-Chip (SoC) designs that provides efficient on-chip communication architecture. It offers scalable communication to SoC and allows decoupling of communication and computation. In NoC, design space exploration is critical due to trade-offs among latency, area, and power consumption. Hence, analytical modeling is an important step for early NoC design. This paper presents a novel top-down approach router model, and utilizes this model for analysis mesh NoC performance measured in terms of throughput, average of queue size, efficiency, and loss and wait time. As case study, the proposed model is used to map a MPEG4 video core to a 4x4 mesh NoC with deterministic routing to measure the overall NoC quality of service. The model is used also to present how much occupancy of average queue size for each router that reduces resources (hardware) area and cost. The accuracy of this approach and its practical use is illustrated through extensive simulation results.